

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Ting, <i>et al.</i>	Attorney Docket:	TSM03-0945
Filed:	Herewith	Examiner:	TBD
Serial No.:	TBD	Art Unit:	TBD
For:	Notched Spacer for CMOS Transistors		

Mail Stop: Patent Application  
Commissioner for Patents  
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Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**


The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of any non-patent literature.

Respectfully submitted,

May 6, 2004  
Date

  
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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	TBD
				Filing Date	Herewith
				First Named Inventor	Ting, <i>et al.</i>
				Art Unit	TBD
				Examiner Name	TBD
Sheet	1	of	1	Attorney Docket Number	TSM03-0945

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
		US-2003/0067045 A1	04-10-2003	Suoiyama et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		GHANI, T. <i>et al.</i> , "100 nm Gate Length High Performance/Low Power CMOS Transistor Structure," IEDM (1999) pp. 415-418.	
		NAKAI, S., <i>et al.</i> , "A 100 nm CMOS Technology with "Sidewall-Notched" 40 nm Transistors and SiC-Capped Cu/VLK Interconnects for High Performance Microprocessor Applications," 2002 Symposium on VLSI Technology Digest of Technical Papers (2002) pp. 66-67.	
		PIDIN, S., <i>et al.</i> , "Experimental and Simulation Study on Sub-50 nm CMOS Design," 2001 Symposium on VLSI Technology Digest of Technical Papers (2001) pp. 35-36.	

Examiner Signature	Date Considered
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

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